Roll No. | | | | | | | | | | | | Total No. of Pages : 2

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BCA (Sem.–2)

DIGITAL CIRCUIT & LOGIC DESIGN

Subject Code : BC-205 (2007 to 2010 Batch)

Paper ID : [B0209]

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains SIX questions carrying TEN marks each and students has to attempt any FOUR questions.**

SECTION-A

1. Write briefly :

   a. What four bit number is equal to its 2's complement?

   b. Discuss the racing condition. How is it avoided?

   c. Compare level triggering and edge triggering.

   d. What is up down counter ?

   e. What are maxterms?

   f. Add a parity bit to make odd parity in the binary word 11001101.

   g. What do you mean by non-weighted codes?

   h. Convert $(0.6875)_{10}$ into octal.

   i. State and prove De-Morgan's Theorem.

   j. What is the difference between latch and flip-flop?

SECTION-B

2. A) Minimize the following logic function and realize using NAND gates :

   f(A,B,C,D)=SIGMA m(l,3,5,8,9,11,15) + d(2,13)

   B) Design a 4-bit carry look ahead adder and explain its truth table for carry generation and propagation.

3. What is the difference between sequential and combinational circuits? Explain the designing of full adder and full subtractor.

4. Write short note on :

   (a) Gate Propagation delay time

   (b) DEMUX

   (c) Code Converter

5. Differentiate between synchronous and asynchronous counters. What is the limitation of parity method for error detection? Describe the Hamming code for error detection and correction.

6. Explain Decoder for binary to gray code.

7. Implement following using 4 x 16 Decoder

   $F = XY + \overline{Z}$